ABSTRACT

A clock doubler including clock doubling circuitry for generating from a system clock a clock signal having a frequency substantially double that of the system clock and also having a pulse width and associated duty cycle is provided. Timing circuitry for generating a first signal indicative of the time the clock signal is low and a second signal indicative of the time the clock signal is high provides an input to comparison circuitry for comparing the first signal and the second signal. Pulse width varying circuitry varies the pulse width of the clock signal based on the result of comparing the first signal and the second signal.